In the Claims:

Please amend claims 1, 2, 4-17, and 19-30. Please cancel claims 3 and 18. The claims are as follows:

1. (Currently Amended) A voltage regulated power supply test circuit, comprising:

a voltage regulator ~~electrically~~ , supplied by an external power supply and having a voltage regulated output directly connected to at least one regulated voltage node of a functional circuit of an integrated circuit chip; and

means for selectively and directly connecting at least one current load circuit between one of said at least one regulated voltage node[[s]] and ground ~~at least one load circuit~~ in response to a control signal ~~adapted to put an emulated current load of said functional circuit on said regulated voltage supply~~.

2. (Currently Amended) The circuit of claim 1, further including a reference voltage generator electrically connected between said voltage regulator and [[a]] said external power supply.

3. (Canceled)

4. (Currently Amended) The circuit of claim 1, wherein said current load circuit comprises a gated resistive load.

5. (Currently amended) The circuit of claim 1, wherein said current load circuit comprises a current mirror.

6. (Currently Amended) The circuit of claim 5, further including means for varying [[the]] an amount of current flowing through said current load circuit.

7. (Currently Amended) The circuit of claim [[6]] 5, wherein said current mirror includes selectable multiple mirror elements each electrically connectable to different voltage sources having different on/off patterns.

8. (Currently Amended) The circuit of claim 1, further including at least one external test ~~point~~ pad, each said at least one external test ~~point~~ pad electrically connected to one of said at least one regulated voltage node[[s]].

9. (Currently Amended) ~~The circuit of claim 8,~~ A circuit for testing a voltage regulated power supply, comprising:

a voltage regulator electrically connected to at least one regulated voltage node of a functional circuit of an integrated circuit chip;

means for selectively connecting between one of said at least one regulated voltage node and ground at least one load circuit adapted to put an emulated current load of said functional circuit on said voltage regulated power supply; and

at least one test point, each said at least one test point electrically connected to one of said at least one regulated voltage node and electrically connected to ~~wherein said one or more test point is~~ an I/O monitor pad of said integrated circuit chip.

10. (Currently Amended) The circuit of claim 9 ~~1, further including~~:

wherein, when there are multiple test points, each test point connected to a different regulated voltage node of said functional circuit; and

said circuit further including means for combining the voltages on each test point into a signal on ~~a one or more~~ said I/O monitor pads~~, a number of said monitor pads being less than a number of said test points~~.

11. (Currently Amended) The circuit of claim 10, wherein said means for combining includes:

a multiplicity of voltage comparators, a first input of each voltage comparator connected to a different test point, a second input of [[said]] each voltage comparator connected to a reference voltage supply, an output of each said comparator connected to inputs of a compression logic and ~~said one or more I/O monitor pads connected to outputs~~ an output of said compression logic connected to said I/O monitor pad.

12. (Currently Amended) The circuit of claim 10, wherein said means for combining includes:

a different test point connected to each input of a multiplexer and an output of said multiplexer connected to an analog to digital converter, said multiplexer and said analog to digital converter responsive to control signals from a control state machine, the output of said analog to digital converter connected to at least one or more I/O monitor pads, said at least one or more I/O monitor pads including ~~of~~ said I/O monitor pad[[s]].

13. (Currently Amended) The circuit of claim 10, wherein said means for combining includes:

a different test point connected to each input of a multiplexer and an output of said multiplexer connected to an analog to digital converter, said multiplexer and said analog to digital converter responsive to control signals from a control state machine, the output of said analog to digital converter connected to a compressed storage device, said compressed storage device responsive to said control signals, and said compressed storage device connected ~~to said one or more of~~ said I/O monitor pad[[s]].

14. (Currently Amended) The circuit of claim [[1]] 9, wherein:

said at least one regulated voltage node[[s are]] is located on a regulated voltage grid;

said functional circuit includes component circuits, each component circuit connected between one of said at least one regulated voltage node and [[a]] at least one ground node on a ground grid having multiple ground nodes; and

each said at least one load circuit also connected to a single ground node of said at least one ground node.

15. (Currently Amended) The circuit of claim 14, further including additional voltage regulators, all said voltage regulators located around a periphery of said integrated circuit chip, each voltage regulator connected to a different regulated voltage node of said ~~one or more~~ at least one regulated voltage node[[s]].

16. (Currently Amended) A method of testing a voltage regulated power supply, comprising:

providing a voltage regulator ~~electrically~~ , supplied by an external power supply and having a voltage regulated output directly connected to at least one regulated voltage node of a functional circuit of an integrated circuit chip; and

selectively and directly connecting at least one current load circuit between one of said at least one regulated voltage node[[s]] and ground, said at least one current load circuit adapted to put an emulated current load on said voltage regulated power supply, said emulated current load emulating a current load of said functional circuit on said voltage regulated ~~voltage~~ power supply.

17. (Currently Amended) The method of claim 16, further including providing a reference voltage generator electrically connected between said voltage regulator and [[a]] said external power supply.

18. (Canceled)

19. (Currently Amended) The method of claim 16, wherein said current load circuit comprises a gated resistive load.

20. (Currently amended) The method of claim 16, wherein said current load circuit comprises a current mirror.

21. (Currently Amended) The method of claim 20, further including varying [[the]] an amount of current flowing through said current load circuit.

22. (Currently Amended) The method of claim [[21]] 20, wherein said current mirror includes selectable multiple mirror elements each having different on/off patterns voltage sources and further comprising selectively connecting one or more [[pf]] of said mirror elements to said current load circuit.

23. (Currently Amended) The method of claim 16, further including providing at least one external test ~~point~~ pad, each said at least one external test ~~point~~ pad electrically connected to one of said at least one regulated voltage node[[s]].

24. (Currently Amended) ~~The method of claim 23,~~ A method of testing a voltage regulated power supply, comprising:

providing a voltage regulator electrically connected to at least one regulated voltage node of a functional circuit of an integrated circuit chip;

selectively connecting between one of said at least one regulated voltage nodes and ground at least one load circuit adapted to put an emulated current load of said functional circuit on said voltage regulated supply; and

providing at least one test point, each said at least one test point electrically connected to one of said at least one regulated voltage node and electrically connected to ~~wherein said one or more test point is~~ an I/O monitor pad of said integrated circuit chip.

25. (Currently Amended) The method of claim 24, ~~16 further including~~:

wherein, when there are ~~providing~~ multiple test points, connecting each test point ~~connected~~ to a different regulated voltage node of said functional circuit; and

further including combining the voltages on each test point into a signal on ~~a one or more~~ said I/O monitor pads~~, a number of said monitor pads being less than a number of said test points~~.

26. (Currently Amended) The method of claim 25, wherein the step of combining includes:

providing a multiplicity of voltage comparators, a first input of each voltage comparator connected to a different test point, a second input of said voltage comparator connected to a reference voltage supply, an output of each said comparator connected to inputs of a compression logic and ~~said one or more I/O monitor pads connected to outputs~~ an output of said compression logic.

27. (Currently Amended) The method of claim 25, wherein the step of combining includes:

providing a different test point connected to each input of a multiplexer and an output of said multiplexer connected to an analog to digital converter, said multiplexer and said analog to digital converter responsive to control signals from a control state machine, the output of said analog to digital converter connected to at least one or more I/O monitor pads, said at least one or more I/O monitor pads including ~~of~~ said I/O monitor pad[[s]].

28. (Currently Amended) The method of claim 25, wherein the step of combining includes:

providing a multiplexer, a different test point connected to each input of said multiplexer, an output of said multiplexer connected to an analog to digital converter, said multiplexer and

said analog to digital converter responsive to control signals from a control state machine, the output of said analog to digital converter connected to a compressed storage device, said compressed storage device responsive to said control signals, and said compressed storage device connected to said ~~one or more of said~~ I/O monitor pad[[s]].

29. (Currently Amended) The method of claim [[16]] 24, wherein;

said at least one regulated voltage node[[s are]] is located on a regulated voltage grid;

said functional circuit includes component circuits, each component circuit connected between one of said at least one regulated voltage node and [[a]] at least one ground node on a ground grid having multiple ground nodes; and

each said at least one load circuit also connected to a single ground node of said at least one ground node.

30. (Currently Amended) The method of claim 29, further including providing additional voltage regulators, all said voltage regulators located around a periphery of said integrated circuit chip, each voltage regulator connected to a different regulated voltage node of said ~~one or more~~ at least one regulated voltage node[[s]].